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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/584,994 | 06/29/2006 | Masaaki Bairo | SON-3173 | 5930 |

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| EXAMINER | |
|---|---|
| KUO, WENSING W | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

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|---|---|
| 09/21/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/584,994 | BAIRO, MASAAKI | |
| | Examiner | Art Unit | |
| | W. Wendy Kuo | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *11 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-8* is/are pending in the application:

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *29 June 2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Ikegami, US 5,973,384.

3. With respect to claim 1, Ikegami teaches a method for manufacturing a bipolar transistor, characterized by comprising:

Forming a base layer 3 on a semiconductor substrate 1 (Figure 5);

Forming in an insulating film 9 stacked on said base layer a base electrode lead opening 9b and an emitter electrode lead opening 9a (Figure 7) at the same time (column 8, lines 40-44; column 10, lines 59-64); and

Subsequently forming a base electrode lead portion (10b, 11b) and an emitter electrode lead portion (10a, 11a) in, respectively, said base electrode lead opening and said emitter electrode lead opening (Figures 12 and 14; column 11, lines 21-36).

FIG.5

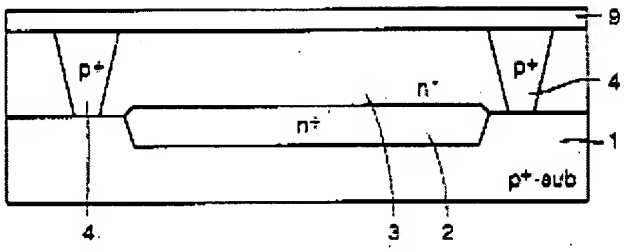



FIG.7

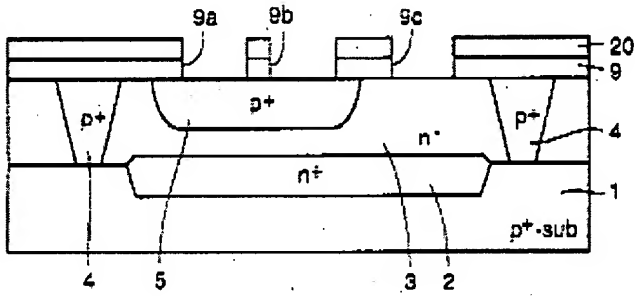
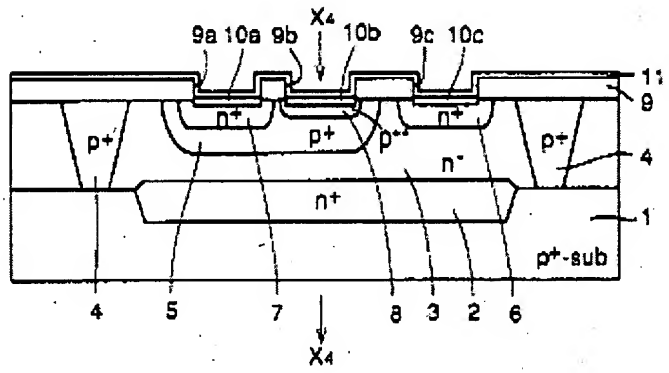



FIG.14

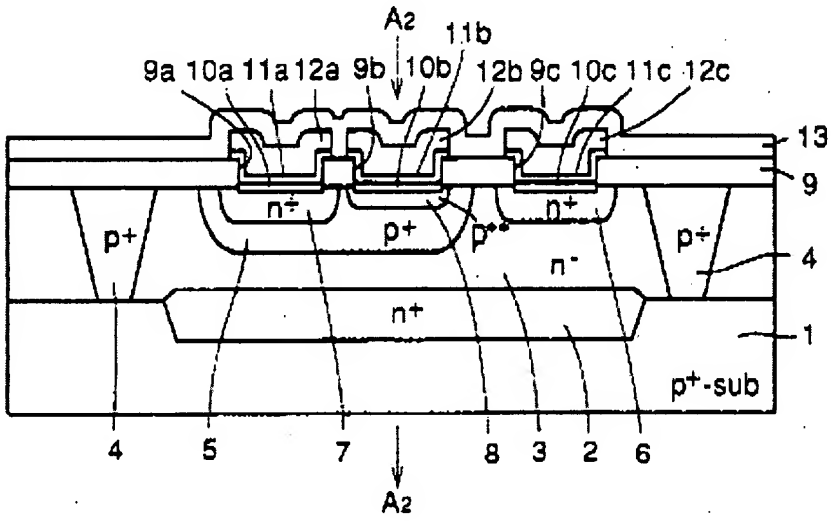



4. With respect to claim 2, Ikegami teaches that the method is characterized in that said base electrode lead portion and said emitter electrode lead portion are formed from the same conducting film 23 at the same time (column 11, lines 21-36).

5. With respect to claim 3, Ikegami teaches in Figure 1 a bipolar transistor having a base electrode lead portion (10b, 11b) consisting of part of a base layer 3 formed on a semiconductor substrate 1, said bipolar transistor characterized in that said base electrode lead portion (10b, 11b) and an emitter electrode lead portion (10a, 11a) are formed in correspondence with, respectively, a base electrode lead opening 9b and an emitter electrode lead opening 9a which are formed at the same time in an insulating film 9 on said base layer 3 (column 8, lines 40-44; column 10, lines 59-64).

*Note that the claim language "which are formed at the same time" is directed to a method of making and does not further limit the structural aspects of the bipolar transistor. Claim language that does not further limit the structure of the device is not patentably distinguishable from the prior art device that has met all of the claimed structural limitations, regardless of the intermediate steps performed to reach the end structure.

*FIG. 1*



6. With respect to claim 4, Ikegami teaches that the bipolar transistor is characterized in that said base electrode lead portion (10b, 11b) and said emitter electrode lead portion (10a, 11a) are formed from the same conducting film (23 Figure 12) at the same time (column 11, lines 21-36).

*Note that the claim language "at the same time" is directed to a method of making and does not further limit the structural aspects of the bipolar transistor. Claim language that does not further limit the structure of the device is not patentably distinguishable from the prior art device that has met all of the claimed structural limitations, regardless of the intermediate steps performed to reach the end structure.

7. With respect to claim 5, Ikegami teaches a method for manufacturing a semiconductor apparatus which has a bipolar transistor having a base electrode lead portion (10b, 11b) consisting of part of a base layer 3 formed on a semiconductor substrate 1 (Figure 1), said method characterized by comprising:

Forming said base layer 3 (Figure 5);

Forming in an insulating film 9 stacked on the base layer 3 a base electrode lead opening 9b and an emitter electrode lead opening 9a (Figure 7) at the same time (column 8, lines 40-44; column 10, lines 59-64); and

Subsequently forming the base electrode lead portion (10b, 11b) and an emitter electrode lead portion (10a, 11a) in, respectively, the base electrode lead opening and the emitter electrode lead opening (column 11, lines 21-36), thus forming the bipolar transistor.

8. With respect to claim 6, Ikegami teaches that the method is characterized in that said base electrode lead portion and said emitter electrode lead portion are formed from the same conducting film 23 at the same time (column 11, lines 21-36).

9. With respect to claim 7, Ikegami teaches in Figure 1 a semiconductor apparatus which has a bipolar transistor having a base electrode lead portion (10b, 11b) consisting of part of a base layer 3 formed on a semiconductor substrate 1, said semiconductor apparatus characterized in that said bipolar transistor has the base electrode lead portion (10b, 11b) and emitter electrode lead portion (10a, 11a) which are formed in correspondence with, respectively, a base electrode lead opening 9b and an emitter electrode lead opening 9a which are formed at the same time in an insulating film 9 on said base layer 3 (column 8, lines 40-44; column 10, lines 59-64).

*Note that the claim language "which are formed at the same time" is directed to a method of making and does not further limit the structural aspects of the bipolar transistor. Claim language that does not further limit the structure of the device is not patentably distinguishable from the prior art device that has met all of the claimed structural limitations, regardless of the intermediate steps performed to reach the end structure.

10. With respect to claim 8, Ikegami teaches that the semiconductor apparatus is characterized in that said base electrode lead portion (10b, 11b) and said emitter electrode lead portion (10a, 11a) are formed from the same conducting film (23 Figure 12) at the same time (column 11, lines 21-36).

*Note that the claim language "at the same time" is directed to a method of

making and does not further limit the structural aspects of the bipolar transistor. Claim language that does not further limit the structure of the device is not patentably distinguishable from the prior art device that has met all of the claimed structural limitations, regardless of the intermediate steps performed to reach the end structure.

***Conclusion***

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Matsumi, US 5,106,769 discloses a process of manufacturing a Bi-CMOS type semiconductor integrated circuit by providing an isolation procedure wherein PMOS and NMOS transistor isolation areas are selectively oxidized so as to form a second isolation oxide film, simultaneous with the selective oxidation of the polysilicon layer deposited on the bipolar transistor area.

Jalali-Farahani et al., US 5,834,800 disclose a heterojunction bipolar transistor in an integrated circuit having intrinsic and extrinsic base portions.

Miwa, US 6,043,552 discloses a bipolar transistor having first and second conductor patterns to prevent an epitaxial layer from contamination by metal when the epitaxial layer is formed on a substrate.

Haynie, US 6,890,826 discloses a method of manufacturing a bipolar junction transistor having an integrated polysilicon base contact and field plate element minimally spaced from a polysilicon emitter contact by using a single mask to define respective openings for these elements.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. Wendy Kuo whose telephone number is (571) 270-1859. The examiner can normally be reached Monday through Friday 7:00 AM to 4:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue A. Purvis can be reached at (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Wendy Kuo

W. Wendy Kuo
Examiner
Art Unit 2826

WWK

LEONARDO ANDUJAR
PRIMARY EXAMINER